An Application of New 3D MCP Packaging Process for Al Wire

Power Devices

Steven Pan

Jiangsu University of Science and Technology, Jiangsu, Zhenjiang, China

Received: October 22, 2024Accepted: November 23, 2024Online Published: November 29, 2024doi:10.22158/asir.v8n4p189URL: http://doi.org/10.22158/asir.v8n4p189

Abstract

Traditional power devices packaging have been low package ratio, and difficult highly about the characteristic of the integrated, can't to adapt to the high integration and high density development trend in the semiconductor packaging industry; In this paper, a new design of Al wire cleaver face, can form a plane on the surface of Al wire or ribbon, realize the second die bond or wire bond on the surface of point. Through the process to achieve the idea that it can be applied to power devices of MCP packaging technology.

Keywords

MCP, Al Wire Bonding, Power Device Packaging

1. Introduction

In recent years, in the semiconductor discrete device industry, China 's packaging and testing enterprises have developed rapidly and steadily. At present, they have occupied a pivotal position in the international market. With the continuous heating up of the electronic machine, consumer electronic products and other markets, in the application of electronic devices such as high power, high back pressure, high frequency and high speed, the market also puts forward higher integration requirements for traditional discrete devices. In order to meet the changing trend of packaging requirements, this paper discusses and studies a new three-dimensional MCP packaging structure that can be realized on discrete devices.

2. Overview of MCP Packaging for Discrete Devices

From the development process of microelectronics. Multi-chip packaging technology (MCP) is a packaging process that can meet the requirements of integrated density and improve the performance of the whole machine (Zhang, 2001). It can be divided into two-dimensional (2D) packaging and

three-dimensional (3D) packaging, but both are a single-package hybrid technology that combines multiple chips in a single plastic packaging shell (Longle, 2006). The discrete semiconductor device is a single unconnected chip with functional characteristics of the device. Electronic device encapsulated in a shell. In order to ensure the product requirements of high power and high current. Discrete devices usually use lead-tin solder to ensure the high conductivity and thermal conductivity of the product. The two-dimensional packaging structure shown in Figure 1 is pasted in two steps. The bonding and encapsulation of aluminum wire or gold wire were carried out in turn. Of course, if the integrated IC chip no conductive thermal packaging requirements. Similarly, IC chips can be stacked on top of another chip using non - conductive adhesive. As shown in Figure 2, the bonding and encapsulation were also completed after high temperature baking.



Figure 1. Two-dimensional Packaging Schematic of Discrete Device MCP

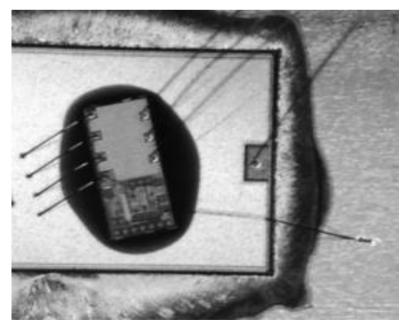


Figure 2. Schematic Diagram of MCP Stacked Packaging for Discrete Devices

3. Analysis of MCP Packaging Structure of Discrete Device

With the continuous development of integrated circuits. The size of the chips that need to be integrated is getting larger and larger. The above two traditional discrete device MCP packaging technology has been unable to meet the higher requirements of the product. Developing new packaging dimensions requires more resources and waste.

How to develop new structures and processes on existing packages to meet customer needs. It has become the primary problem that needs to be solved urgently in the MCP packaging process of discrete devices.

3.1 Two-dimensional Packaging Structure Analysis

The two-dimensional packaging discrete device secondary chip product by lead-tin wire process. The distance between the two chips is too close, which will lead to the fusion of tin beads during the tinning process. As a result, the amount of tin overflow around the small chip U2 is insufficient, so the U1 and U2 chips need to maintain a chip spacing of at least 0.8 mm. At the same time, considering that the chip is too close to the edge of the frame base island. It will also lead to the problem that the rear aluminum wire bonding claw cannot be placed and the solder overflows the side of the frame base island. Therefore, the distance between the chip and the edge of the frame base island needs to be set aside more than 0.5mm. Therefore, the packaging ratio of two-dimensional packaging structure is seriously limited, which cannot meet the increasing packaging requirements of chip size.

3.2 Stacked Package Structure Analysis

Adopts stacked packaging discrete device products, and the top chip will occupy a large amount of surface pressure area space of the bottom chip. When the on-current IDS of discrete power devices is small, only a thick aluminum wire is usually needed to connect the pad of the chip and the lead frame. However, with the increasing demand for current processing capability of power devices. The conduction current of the device becomes larger and larger. At this time, a thick aluminum wire is not enough to conduct higher and higher currents, and multiple thick aluminum wires or thicker aluminum wires will be used to meet product requirements. After using the stacked packaging structure design. The weldable area on the bottom chip surface can not meet the welding requirements of the product.

4. Packaging Structure and Process Optimization

The main problem of the MCP packaging structure is the design of the internal space of the package, that is, the use of stacked packaging structure without affecting the electrical requirements of the product. Aluminum wire solder joints with high space ratio can be utilized. Adhesively on its surface twice.

However, it is necessary to consider the height of the packaging structure, the design of the end face of the steel nozzle and the feasibility of the process flow.

4.1 Packaging Structure Height Problem

At present, the discrete device packaging mainly includes TO-220, TO-247, TO-252 and other structures. From the discrete device packaging altimeter shown in Table 1, it can be seen that the packaging height is above 1800 um after deducting the frame thickness.

Deduct 250 um conventional solder joint height. The remaining height is above 1500 um, and the conventional chip thickness is 300 um. After deducting the height of the two chips, the 900 um height design can meet the arc height requirements of the welding wire.

Encapsulated type	Packaging height	Base island frame	Aluminum wire /	Remaining height
	(um)	thickness (um)	strip thickness (um)	(um)
TO-247	5000	1980	250	2770
TO-220-3L-C	4500	1300	250	2950
TO-252-4R	2300	500	250	1550

Table 1. Discrete Device Package Altimeter

4.2 Aluminum Wire / Strip Mouth Wedge end Face Design Improvement

The end face of the aluminum wire / strip mouth wedge is designed to be V-shaped and the bottom is not flat. As shown in Figure 3, the upper surface of the welding point after the completion of the welding line is a narrow rectangular shape. Convex. It cannot be reused such as dispensing or welding. Without changing the interface space of the wedge side. The V-shaped end face of the aluminum wire steel nozzle wedge is changed to a trapezoid. At the same time, the height of the trapezoid is reduced and the width of the upper edge of the trapezoid is increased. The shape of the welding line can be optimized. Finally, a platform of standard rules is created above the welding point. It can be used for secondary use such as dispensing or welding as shown in Figure 4. The thrust test strength of the pin solder joint of the re-designed product meets the standard requirements. The solder joint area on the surface of the chip was rotten ball test without crater and pressure zone damage.

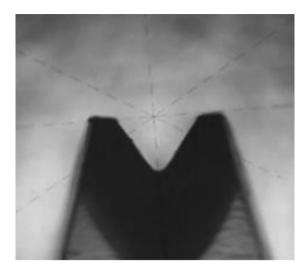


Figure 3. Aluminum Wire Wedge Tool with V-shaped End Face



Figure 4. Aluminum Wire Wedge Tool with Trapezoidal End Face

4.3 Process Optimization Design

The U1 chip is still bonded by the lead-tin wire process. The chip volume only needs to consider that the distance between the chip and the edge of the frame base island needs to be set aside more than 0.5mm, and the packaging ratio is greatly optimized. After the U1 chip is bonded, the aluminum wire bonding is carried out, and the position of the aluminum wire solder joint on the chip surface is optimized. The distance between the solder joints can be adjusted according to the size of the U2 chip to complete the adhesion of the U2 chip. According to the glue type, the baking is completed in the oven, and the ball welding of the gold wire or copper wire is finally completed. The profile diagram is shown in Figure 5. The appearance and electron microscope diagram of the finished product after packaging are shown in Figure 6 and Figure 7.

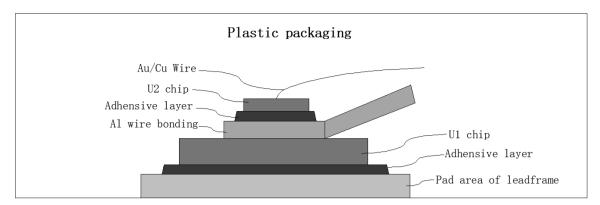


Figure 5. Plastic Sealing Body Section Diagram

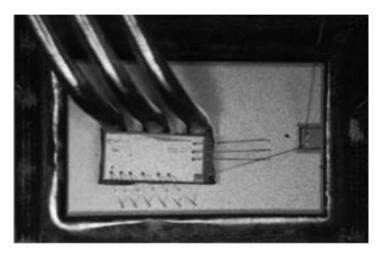


Figure 6. Secondary Mounting Product Appearance Diagram

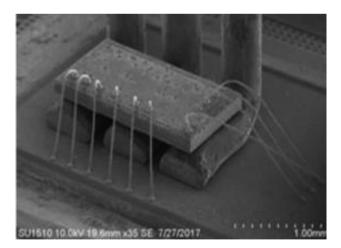


Figure 7. Electron Microscope Diagram of Secondary Mounting Products

5. Batch Production Results

After the re-optimization design of the packaging structure and process flow, the problem of limited size of the U1 chip of the discrete device MCP package is solved, and the problems of lead-tin overflow at the edge of the lead frame base island, less tin under the chip, and chip edge damage (bonding jaw crush) are greatly reduced. At the same time, the electrical output of the product is guaranteed. After 20,000 productions, the product packaging yield is as high as 98 %, and the product yield is increased to more than 97 % after product testing. No fluctuations in packaging yield and test yield were found among multiple batches, and it was believed that the packaging structure and process design were optimized.

6. Conclusion

The results of MCP packaging structure and process optimization of semiconductor discrete devices show that. The problem of limited packaging ratio of discrete devices is effectively solved by secondary bonding on the surface of aluminum wire solder joints. The process problems such as lead-tin overflow at the edge of the lead frame base island and less chip tin are eliminated.

References

- Longle. (2006). Multichip Packaging Technology and Its Application. *Electronics and Packaging*, 6(1), 12-15.
- Zhang Guangyuan. (2001). Prospects of Single Chip Packaging and Multichip Packaging. *Electronics* and Packaging, 1(1), 11-15.