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Original Paper

The Roadmap and Manufacturing Challenges of EMLs and CW Lasers for 800G, 1.6T, and 3.2T Super Intelligence (SI) and Artificial Intelligence (AI) Computing Applications

Jack Jia-Sheng Huang[1,2*]

[1] Source Photonics, 8521 Fallbrook Avenue, Suite 200, West Hills, CA 91304, USA

[2] Source Photonics, No.46, Park Avenue 2nd Rd., Science Park, Hsinchu, Taiwan

[*] Corresponding author: Dr. Jack Jia-Sheng Huang, Chip BU CEO and Fab GM, Source Photonics, 8521 Fallbrook Avenue, Suite 200, West Hills, CA 91304, USA. E-mail: jack.huang@sourcephotonics.com

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Abstract

This paper presents the roadmap and manufacturing challenges of electroabsorption-modulated lasers (EMLs) and continuous-wave (CW) lasers for 800G, 1.6T, and 3.2T super intelligence (SI) and artificial intelligence (AI) optical transmission and computing applications. We highlight the roadmap for EMLs and CW lasers across different generations of optical switching technologies and discuss key manufacturing challenges, including (1) technical complexity, (2) substrate constraints, and (3) process equipment requirements.

Keywords

Artificial intelligence, AI, Super intelligence, SI, electro-absorption modulated laser, EML, continuous-wave (CW) laser, 400G, 800G, 1.6T, 3.2T

Introduction

Electro-absorption modulated lasers (EMLs) and continuous-wave (CW) lasers are indispensable semiconductor lasers for super intelligence (SI) and artificial intelligence (AI) optical communication systems (Okuda et al., 2021; Huang et al., 2024; Honda et al., 2023; Zhou et al., 2022; Aoyama et al., 2024; Johnson et al., 2022). EMLs combine the functions of a laser diode (LD) and an electro-absorption modulator (EAM) in a single device, enabling high extinction ratio (ER) and high-speed operation. Owing to their low chromatic dispersion, EMLs offer performance advantages

over directly modulated lasers (DMLs) and remain a mainstream laser source for high-speed optical transmission at 100G, 200G, 400G, and 800G. Optical output signals are generated by applying ON/OFF electrical signals to the EAM section without directly modulating the LD current or significantly altering the properties of the laser diode section (Huang et al., 2024).

Beyond 800G, CW laser-based silicon photonics is becoming increasingly popular due to advantages such as low cost and low power consumption (Zhou et al., 2022; Aoyama et al., 2024; Johnson et al., 2022). The cost advantage is particularly pronounced for DR4, which requires only one wavelength (1310 nm). For example, each 800G 2×DR4 optical transceiver module requires one to two 1310 nm CW lasers to power the photonic integrated circuit (PIC) modulators, while eight 53 Gbaud (100G PAM4) EMLs are required to transmit signals across eight lanes.

SI and AI play vital roles in reasoning, medicine, healthcare, weather forecasting, and many other applications. Since the launch of ChatGPT in November 2022, AI has emerged as a modern industrial revolution (Lock, 2022). ChatGPT helps users obtain answers, access useful references, and enhance productivity. Following the release of NVIDIA's DGX H200 supercomputing systems in 2023, AI infrastructure and AI factories have been reshaping and transforming various industries (Fibermall, 2023). In early 2025, the introduction of DeepSeek language models further accelerated the integration of AI tools into everyday applications through accessible platforms (Ng et al., 2025; Goldman et al., 2025). In September 2026, the term "super intelligence" gained increasing attention among President Trump, AI industry leaders, and policymakers (Eliot, 2026; Ahn, 2026). Today, SI has expanded into physical AI applications such as autonomous vehicles, robotics, and unmanned fighter jets.

SI/AI roadmap and optical devices

Figure 1 illustrates the roadmap of lasers and optical modules over the past decade. The demand has been driven primarily by the data center and AI waves. During the recent AI wave, demand for 800G, 1.6T, and beyond has grown exponentially (Kozlov, 2023). High-speed optical links, such as 800G and 1.6T optical transceivers, enable SI/AI systems to rapidly exchange information and process data. AI tokens, which are units of data processed by AI models, are generated during training and inference and enable prediction, generation, and reasoning (Salvator, 2025).

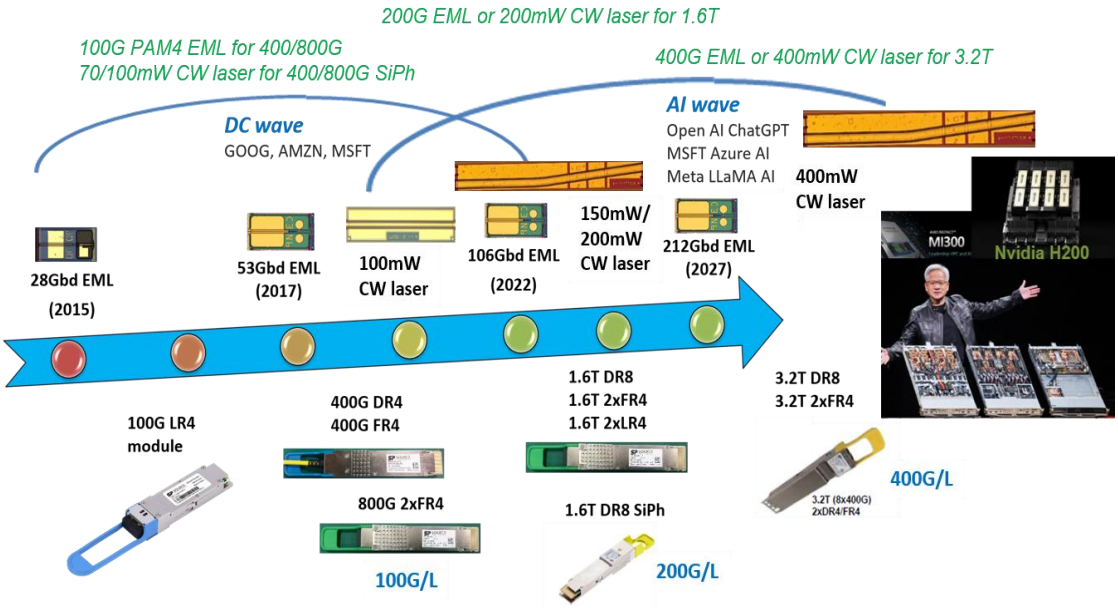


Figure 1. Evolution of EMLs and CW lasers and their corresponding optical transceivers for SI/AI applications at 400G, 800G, 1.6T, and 3.2T.

Figure 2 illustrates two AI infrastructure architectures for various optical communication schemes ranging from 400G to 3.2T. In the AI infrastructure industry, Scale-Up and Scale-Out refer to two different approaches to increasing AI computing capacity (Gavin, 2025; Wallner, 2025; Lorame, 2026). This distinction is becoming increasingly important because it directly drives the demand for EMLs, silicon photonics, optical interconnects, and co-packaged optics (CPO).

AI Scale-Out means connecting multiple GPU clusters to build a much larger AI system. An analogy for AI scale-out is increasing compute capacity by building multiple supercomputers and connecting them through Ethernet or InfiniBand networks. Scale-out can be viewed as horizontal or cluster expansion.

AI scale-out represents a major market today, where optical modules such as 400G DR4, 800G DR8, 800G 2×FR4, 1.6T DR8, and 1.6T 2×DR4 are heavily deployed by major hyperscale cloud service providers (CSPs) such as Meta, Microsoft, Google, and AWS.

The technologies used include 100G EML, 200G EML, 100 mW CW laser, 150 mW CW laser, and 200 mW CW laser. In addition to the 1310 nm wavelength used for DR4, the wavelength range also extends to coarse wavelength division multiplexing (CWDM) for FR4 and LAN-WDM (LWDM) for LR4.

AI Scale-Up means increasing computing power within a single AI cluster or training domain, similar to enhancing the capacity of a single supercomputer. AI scale-up infrastructure uses active optical cables (AOCs), CPO, and external laser small form factors (ELSFPs) to replace copper cables.

Companies such as Nvidia, Broadcom, and Marvell are investing heavily in optical scale-up fabrics. The technologies include ultra-high-power (UHP) 400 mW CW lasers, silicon photonics photonic integrated circuits (PICs), and CPOs to enable vertical local integration.

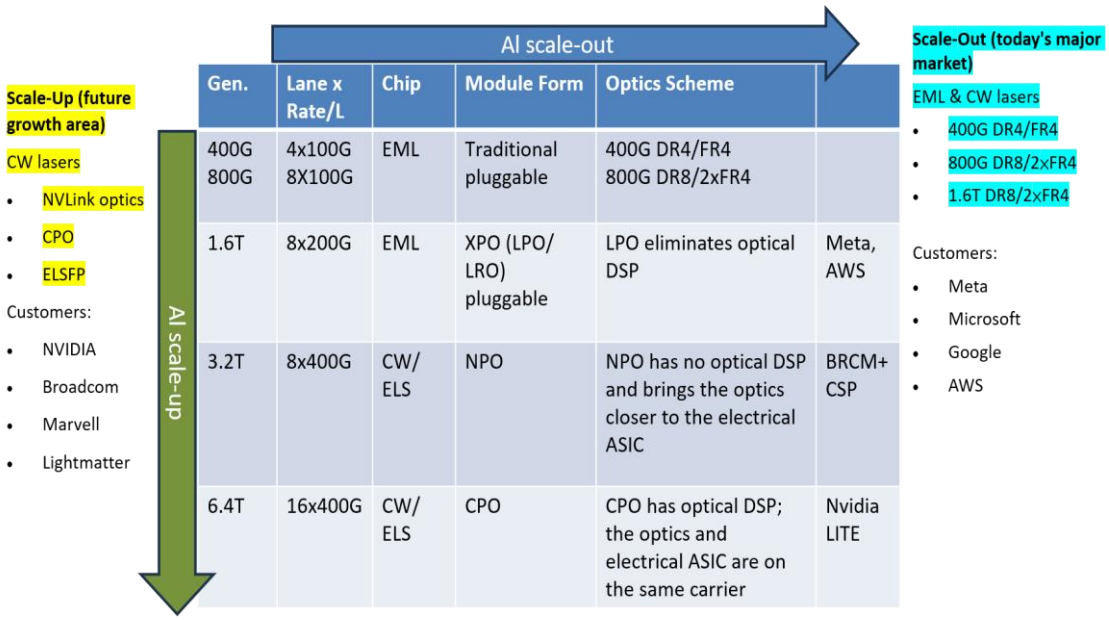


Figure 2. AI scale-out and scale-up roadmaps for EMLs and CW lasers in SI/AI applications at 400G, 800G, 1.6T, 3.2T, and 6.4T. AI scale-out is the mainstream technology, while AI scale-up is an emerging technology.

Optoelectronic laser fabrication

Figures 3(a) and (b) show the three-dimensional schematics of the monolithically integrated EML structure and CW laser, respectively. In the EML device shown in Fig. 3(a), the front section serves as the modulator for RF modulation, while the rear section consists of a distributed feedback (DFB) laser that acts as the light source. The LD and EAM are monolithically integrated using butt-joint (BJ) technology (Huang et al., 2023; Zhou et al., 2022), in which the EAM is regrown adjacent to the LD. These two sections are separated by an isolation region.

For both the LD and EAM, quaternary InGaAsP multi-quantum-well (MQW) and separate-confinement heterostructure (SCH) layers were grown using metal-organic chemical vapor deposition (MOCVD). A SiO_2 dielectric layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) for passivation. Contact openings were formed in the dielectric layer to establish Ohmic contact with the Ti/Pt/Au p-metal (Huang et al., 2023).

In the CW laser shown in Fig. 3(b), the entire device consists of a DFB laser section that emits high optical power into the PIC modulator. Signal modulation is achieved by external PIC components.

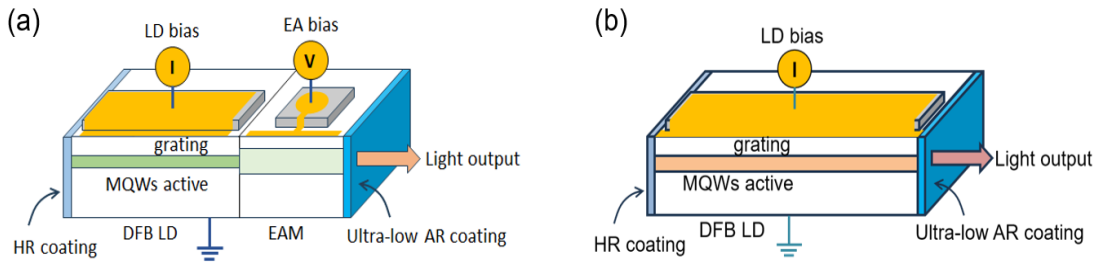


Figure 3. 3D schematics of (a) the EML device structure and (b) the CW laser. In the EML, signal modulation is applied to the front EAM section to modulate the optical signal generated by the rear LD section, which operates under CW bias conditions. For the CW laser, the LD emits optical power into the external PIC for modulation.

Wafer qualifications

Figure 4 shows the general fabrication flow of the EML. Step 1 is the base-wafer epitaxial growth of the MQW and SCH layers, collectively referred to as the active region. Step 2 is holographic or nanoimprint lithography (NIL) grating, which defines the lasing wavelength and enables single-mode operation. Step 3 consists of four regrowth steps: grating overgrowth, butt-joint regrowth, window-facet regrowth, and final regrowth.

Steps 4–7 are the front-end processes performed before wafer thinning, collectively referred to as Process A. These steps include tens to hundreds of photolithography, etching, cleaning, and rinsing processes to create the LD and EAM ridge structures.

Steps 8–9 are the front-end processes performed after wafer thinning, collectively referred to as Process B. These steps include wafer lapping, backside n-metal deposition, and wafer-to-bar cleaving.

After wafer processing (Steps 4–8), the wafers are cleaved into laser bars (Step 9), which are immediately coated with ion-beam-sputtered (IBS) films (Step 10). The front facet of each EML is coated with an ultra-low-reflectivity antireflective (AR) coating to minimize optical reflection, while the rear facet is coated with a highly reflective (HR) coating.

In Step 11, individual chips are scribed from the laser bars and then tested for light versus current (LI), current versus voltage (IV), and optical spectrum (Step 12), followed by a final automated optical inspection (AOI) to check the top surface, front facet, and rear facet of the laser.

	MOCVD epi								
EML	1	2	3.1		3.2		3.3		3.4
	Base MQW growth	Grating	Grating overgrowth	Butt-joint process	Butt-joint regrowth	Window facet	Window facet regrowth	Align key	Final regrowth
Wafer qual	level-1	level-1	level-1	level-1	level-1	level-2	level-1	level-4	level-2
	Process-A								
	4	5		6		7			
	Transfer key	Ridge photo & etch	LD-EA isolation	SiN_x/oxide deposition	SiN_x/oxide contact opening	Ti/Pt/Au p-metal	Chip ID	Au plating	Street open
Wafer qual	level-4	level-3	level-3	level-3	level-3	level-3	level-4	level-3	level-4
	Process-B			Back-end					
	8		9	10		11		12	12.2
	Lapping & polish	N-metal	Bar cleaving & coating	AR & HR coating	OM	Chip scribing	OM	Chip testing	AOI
Wafer qual	level-3	level-3	level-3	level-2	level-4	level-4	level-4	level-4	level-4

Figure 4. General guidelines for wafer qualification at each process step of EML fabrication.

Figure 5 shows the general fabrication flow of the CW laser. The fabrication flow is similar to that of the EML, except for the MOCVD base-wafer structure, regrowth steps, and process designs. For the CW laser, there are three regrowth steps (grating overgrowth, blocking regrowth, and final regrowth) for the buried heterostructure (BH) and two regrowth steps (grating overgrowth and final regrowth) for the ridge waveguide (RWG).

Steps 4–7 (Process A) are the front-end processes performed before wafer thinning to create the BH structure. Steps 8–9 (Process B) are the front-end processes performed after wafer thinning.

In Step 10, the laser bars are immediately coated with IBS films. The front facet of each CW laser is coated with an AR coating to minimize optical reflection, while the rear facet is coated with a HR coating. In Step 11, individual chips are scribed from the laser bars and then tested for LI, IV, and optical spectrum (Step 12), followed by a final AOI to check the visual appearance of the laser.

	MOCVD epi								
CW laser	1	2		3.1			3.2		3.3
	Base MQW growth	Grating	CPM	Grating overgrowth	Stripe definition	Mesa etch	Blocking regrowth	Stripe removal	Final regrowth
Wafer qual	level-1	level-1	level-1	level-1	level-3	level-2	level-2	level-3	level-2
	Process-A								
	4	5		6		7			
	Transfer key	Channel photo	Channel etching	Passivation	Passivation opening	Ti/Pt/Au p-metal	Chip ID	Au plating	Street open
Wafer qual	level-4	level-3	level-3	level-3	level-3	level-3	level-4	level-3	level-4
	Process-B			Back-end					
	8		9	10		11		12	12.2
	Lapping & polish	n-metal	Bar cleaving	AR & HR coating	OM	Chip scribing	OM	Chip testing (CT)	AOI
Wafer qual	level-3	level-3	level-3	level-2	level-4	level-4	level-4	level-4	level-4

Figure 5. General guidelines for wafer qualification at each process step of CW laser fabrication.

Table 1 summarizes the device speeds and transmission formats of EMLs and CW lasers for various AI applications ranging from 400G to 3.2T. At present, 100G-per-lane, or 53-Gbaud, EMLs remain the mainstream components for high-speed optical transceivers. By using 100G-per-lane lasers, chip and transceiver suppliers can meet cost and performance targets for 400G and 800G optical switching applications.

However, for 1.6T and beyond, CW lasers are expected to offer several advantages, including lower cost, lower power consumption, and greater scalability (Shekhar et al., 2024; Hurtt et al., 2007). In addition, CW lasers and PICs hold greater promise for integration with CPO and future roadmap extensions.

Table 1. High-speed lasers and optical transceivers for the evolution from 400G to 3.2T.

Optical transceiver	400G	800G	1.6T	3.2T
Date rate/lane	100G	100G (dominant) 200G (alternative)	200G	400G
Transmission	4x100G PAM4	8x100G PAM4 or 4x200G PAM4	8x200G PAM4	8x400G PAM4
EML scheme	53Gbd EML	53Gbd EML (dominant) 106Gbd EML (alternative)	106Gbd EML	212Gbd EML
Silicon photonics scheme	70mW CW laser + PIC	100mW CW laser + PIC	150mW/200mW CW laser + PIC	400mW CW laser + PIC

Table 2. Wafer qualification requirements for EMLs and CW lasers, categorized from Level 1 to Level 4.

Wafer Qual	EML	CW laser
Level-1	5000-hour aging	5000-hour aging
Level-2	2000-hour aging	2000-hour aging
Level-3	500-hour accelerated life test (ALT)	500-hour accelerated life test (ALT)
Level-4	Burn-in	Burn-in

Table 2 shows the definitions of Level 1 through Level 4 wafer qualifications. Level 1 qualification involves major design, process, and engineering changes that require 5,000-hour aging tests to validate reliability performance. Examples of such major changes include MOCVD MQW growth, grating formation, butt-joint regrowth, and window-facet regrowth, as shown in Figs. 4 and 5.

Level 2 involves changes in final regrowth and optical coating that require 2,000-hour aging verification. Level 3 typically employs a quick 500-hour accelerated life test (ALT) to validate non-critical process changes, such as ridge etching, isolation etching, passivation deposition, p-metallization, and n-metallization. Level 4 qualification is a burn-in screening process applied to 100% of wafers and devices.

Burn-in and reliability aging data were collected from chip-on-submount (CoS) samples. The chips were electrically connected to the submounts using wire bonding. The aging test was conducted at a stress current of 120 mA and a case temperature of 85 °C. The ALT was conducted at a stress current of 200mA and a case temperature of 100 °C. All EML devices were screened for burn-in, and 32 samples were selected from the wafer for reliability aging testing.

Manufacturing challenges

Table 3 summarizes the manufacturing challenges for EMLs and CW lasers. **Challenge 1** is the substrate constraint. Due to the limited supply of InP substrates, meeting hyperscale demand has become increasingly challenging. **Challenge 2** is MOCVD epitaxial uniformity in MQW base growth and EA BJ regrowth. For 100G and 200G EMLs, even small variations in MQW thickness and composition can affect power, ER, and SMSR. In addition, smaller device geometries can also increase sensitivity to BJ interface defects, regrowth protrusions, and optical coupling loss between the LD and EAM sections. **Challenge 3** is DFB grating uniformity. The specification for grating uniformity has become increasingly stringent due to the tight design windows required to achieve high power, high ER, and high SMSR.

Challenge 4 is the high-power requirement, particularly at 200G/lane and 400G/lane. **Challenge 5** is the high-ER requirement, particularly at 200G/lane and 400G/lane. The tradeoff between ER and optical power resulting from detuning makes it more difficult to achieve both high power and high ER.

Challenge 6 is the high-SMSR requirement, which is also more stringent for 200G/lane and 400G/lane. **Challenge 7** is the process complexity and difficulty associated with device shrinking and multi-level stacking. For the latter, multi-level stacking structures, such as sandwiched SiNx/SiO2 passivation layers, are employed to enhance the hermetic performance of EMLs. For the former, device shrinking, such as reducing the length and width of the EA section, makes alignment more difficult. The overlay specification is typically less than 0.5 μm, requiring high-resolution steppers and specialized skill sets to achieve.

Challenges #1 and #7 are related to supply chain constraints, representing common bottlenecks faced by the industry. For example, global demand for 3-inch InP substrates is forecasted to exceed 2 million, 3 million, and 4 million wafers in 2026, 2027, and 2028, respectively (Trend Force, 2026). Such high substrate demand (Challenge #1) represents more than a tenfold increase compared with historical demand.

The process equipment associated with Challenge #7 is also becoming increasingly critical, as many optoelectronic chip suppliers are ramping up their fab capacities. It is therefore important to increase wafer throughput for processes such as PECVD, reactive ion etching (RIE), and photolithography (Oxford, 2026). Long lead times and supply constraints are the main bottlenecks for process equipment delivery.

MOCVD epitaxial uniformity across the wafer (Challenge #2) is critical to the performance and yield of EML and CW laser chips. Good uniformity in photoluminescence (PL) intensity and PL wavelength is important for material quality and device reliability (Huang et al., 2024; Huang et al., 2023).

Grating uniformity (Challenge #3) is critical to threshold current, optical power, ER, single-mode DFB wavelength, and SMSR. In addition to affecting performance and yield, the grating may also impact device reliability (Huang et al., 2023).

Good control of the substrate, MOCVD epitaxial wafer, grating, and fabrication processes significantly affects the power, ER, and SMSR performance associated with Challenges #4, #5, and #6 (Huang et al., 2025).

Table 3. Manufacturing challenges for EMLs and CW lasers.

Challenges	EML	CW laser
Substrate	InP substrate constraint	InP substrate constraint
MOCVD epi	(1) Base MQW epi control (such as PL across the 3” wafer) (2) Butt-joint (BJ) regrowth control	(1) Base MQW epi control (such as PL across the 4” wafer) (2) Blocking regrowth profile
DFB grating uniformity	Grating pitch and duty cycle uniformity	Complex grating uniformity
High power	Yield stability for high power (>12mW) for 200G PAM4 and 400G PAM4 EMLs	Yield stability for high power (>200mW and >400mW) CW lasers

High ER	Yield stability for high ER (>7.5dB)	Typically not screened for ER
High SMSR	Yield stability for high SMSR (>45dB)	Yield stability for high SMSR over temperature and bias
Process	Tighter critical-dimension (CD) control, overlay accuracy, and etch uniformity	Laser facet coating quality and uniformity to prevent catastrophic optical damage (COD)

Conclusions

This paper has reviewed the roadmaps and manufacturing challenges of EMLs and CW lasers for 800G, 1.6T, and 3.2T SI/AI optics. AI scale-out and scale-up infrastructures, along with the corresponding devices and optical modules, have been discussed. The types of EMLs and CW lasers deployed in 400G, 800G, 1.6T, and 3.2T applications have also been presented.

We have also proposed wafer-level qualification guidelines for EMLs and CW lasers. For the most critical MOCVD growth, process, and regrowth steps, Level 1 qualification with 5,000-hour aging is required to qualify the wafers. For Level 2 qualification, 2,000-hour aging is used for wafer validation. For most processes, Level 3 qualification with a 500-hour ALT is employed to provide rapid feedback.

Finally, we have identified seven key manufacturing challenges for EML and CW laser fabrication. The main challenges include (1) InP substrate supply, (2) MOCVD epitaxial uniformity, such as PL wavelength and PL intensity, (3) DFB grating uniformity, (4) high-power requirements for 100G EMLs, 200G EMLs, and 100 mW and 200 mW CW lasers, (5) high-ER requirements for 100G and 200G EMLs, (6) high-SMSR requirements for 100G and 200G EMLs, and (7) process equipment lead times and supply constraints.

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